Performance Improvement of QPSK Modem with AWGN Implemented in FPGA

Umesharaddy1, B.K.Sujatha2

Abstract: This paper presents the methods to design optimized QPSK MODEM with AWGN. The Proposed methods consume less time, power and give better throughput using Spartan-3 and Sparatn-6 FPGA boards. The whole module is divided into several sub modules and those modules are designed using the verilog HDL. Finally, these modules are invoked and integrated to design top level module. Here, two different approaches are used to design the QPSK modulator and they are compared with a conventional QPSK modulator which is designed using arithmetic multipliers and adders. In one of the proposed methods, the modulator is designed by using Vedic multiplier and carry look-ahead adder and demodulator is designed using an FIR LPF with AWGN. The FIR LPF coefficients are generated in MATLAB using a rectangular window and hamming window with AWGN. In the second method, QPSK modulator is designed using multiplexers. The QPSK module is implemented on Spartan-3 and Spartan-6(Atlys) FPGA board. The whole system has been simulated in Xilinx 14.7 and implemented on to the chips XC3S400-4pq208 and XC6SLX45 - CSG324. The results show that the proposed methods can greatly improve the speed and reduce the latency and improve the frequency of operation.

Keywords: *QPSK, FPGA, MODEM, HDL, AWGN, SDR, FIR.*

I. INTRODUCTION

The advancements in wireless communication technology using various digital modulation techniques to transmit data with extreme low power have led us to use the concept of software defined radio (SDR). The process, where more and more hardware components are replaced with software, has resulted in coining the term SDR - because if the components can be replaced with software, then indeed the very functionality of these components can be redefined by using this software. By writing a new program module, a software radio is able to interoperate with different wireless protocols, incorporate new services, and upgrading to new standards.

Present software-defined radios (SDR) employ front end circuits that contain multiple receivers and transmitters for each band of interest, which is inflexible, expensive and power inefficient [4]. A programmable front end circuit is implemented on a CMOS device and is configurable to transmit and receive signals in a wide band of frequencies, thereby providing an adaptable transmitter and receiver operable with current and future wireless networking technologies. In this paper, the FPGA implementation of QPSK modulator using two different methods, i.e., proposed method-1 and proposed method-2[1] and comparison with the conventional QPSK modulator method is done and also demodulator design for proposed method-1 is presented with AWGN [16]. Complete modulator and demodulator units are modeled using Verilog and functionality is verified using I-Sim simulation tool [6] [11]. The code is synthesized fully onto Xilinx FPGAs.

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II. CONVENTIONAL QPSK MODULATOR

In this method the input 16 bit stream is divided into even and odd components of 8-bits each. These even and odd components are multiplied with cosine and sine waves respectively using normal arithmetic multiplier and finally these In phase and Quadrature phase components are added using normal arithmetic adder as shown in Figure 1.

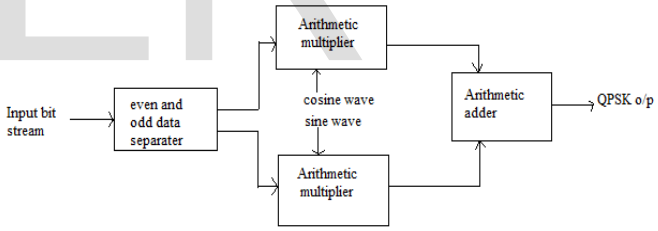

Figure 1. Proposed conventional QPSK modulator.

III. PROPOSED METHOD-1 QPSK MODEM WITH AWGN

Proposed Method - 1 of QPSK modulator is designed by using Vedic multiplier (VM) and Carry Look Ahead adder (CLA) [2]. The input bit stream is divided into even and odd bits and multiplied by cosine and sine wave respectively using Vedic multiplier instead of normal arithmetic multiplier and later adding the in phase and quadrature phase component using carry look-ahead adder instead of normal arithmetic adder as shown in Figure 2[3].

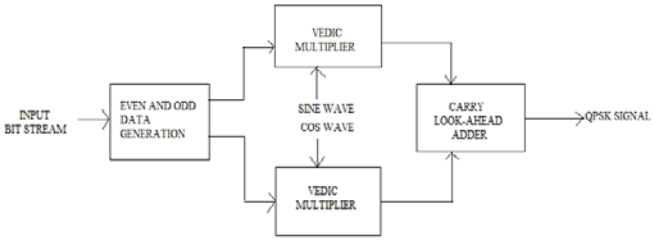

Figure 2. Proposed Method-1 QPSK Modulator

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed and also 4-bit carry look ahead adder is implemented to reduce the ripples of carry so that performance can be improved shown in Figure 3.

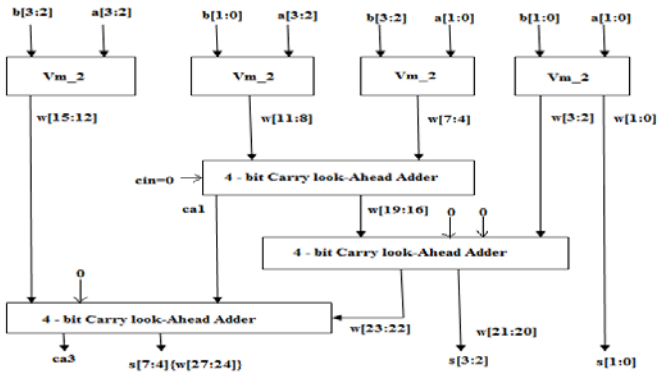

Figure 3. 4 Bit Vedic Multiplier

Similarly using 4-bit vedic multiplier 8-bit vedic multiplier can be designed and using 8-bit vedic multiplier 16-bit vedic multiplier can also be designed and so on as shown in the Figure 4 and Figure 5 below [8].

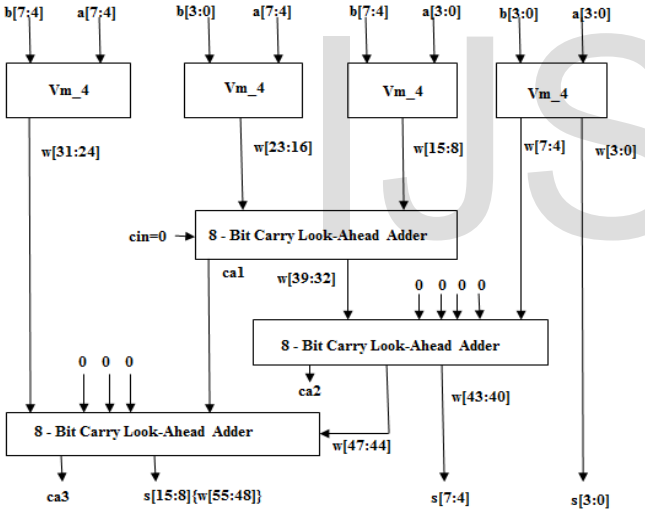

Figure 4. 8 Bit Vedic Multiplier

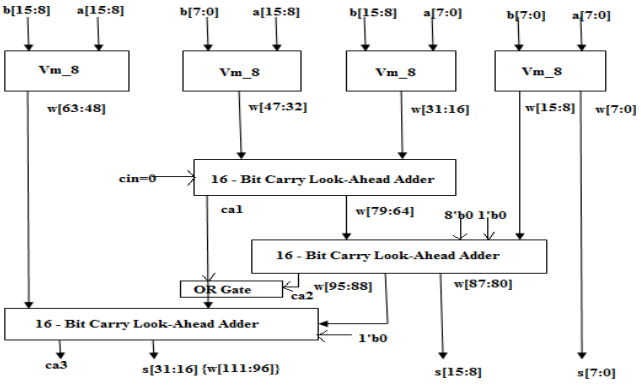

Figure 5. 16 Bit Vedic Multiplier

A. PROPOSED METHOD-1 QPSK DEMODULATOR WITH AWGN:

The previously designed Vedic multiplier and CLA blocks as described previously are used in designing the QPSK demodulator module along with FIR (Finite impulse response) Low pass filter designed using Hamming window with AWGN as shown in Figure 6.

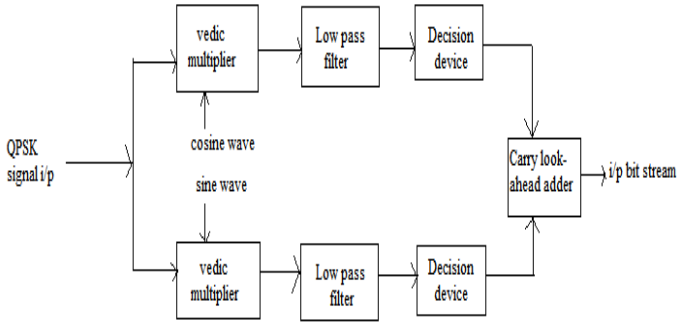

Figure 6. QPSK Demodulator for Proposed method-1 with AWGN

B. PROPOSED METHOD-2 OF QPSK MODULATION

For the second QPSK modulator architecture, the above proposed QPSK modulator 1 architecture will be constructed just to collect four different combinational input data for different phases of QPSK. Once the data is collected, the first proposed QPSK modulator architecture will not be used for future method. In this method, data for each QPSK is collected and stored in four different ROM blocks. Each ROM will store data for one QPSK phase. Since all the four possible phases for a QPSK is stored in four different ROM's, the digital QPSK modulator is no longer required to produce a QPSK phase from I and Q phase as in first method QPSK modulator[18]. For the simulation purposes, a serial input sequence will be considered as input to the 1:2 demultiplexer. The 1:2 demultiplexer will separate the input sequence into odd and even bits. These odd and even bits will be the input for the 4:1 multiplexer which will select one ROM for different combination of odd and even bits as shown in Figure 7.

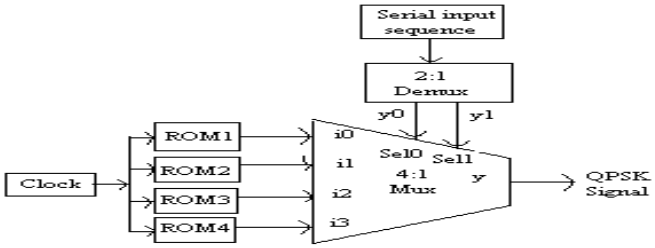

Figure 7. Block diagram for 2nd proposed QPSK modulator

In this modulation technique the input sixteen bit data bit stream is divided into two bits at a time. These two bits 00,10,01,11 act as the select lines for the multiplexer which selects sine with 0 degree, sine with 90 degree, sine with 180 degree and sine with 270 degree phase shifts respectively. Then all these are concatenated to get the final QPSK wave.

Below Figure 8 shows implementation of QPSK modulator with elaboration using multiplexer concept[10].

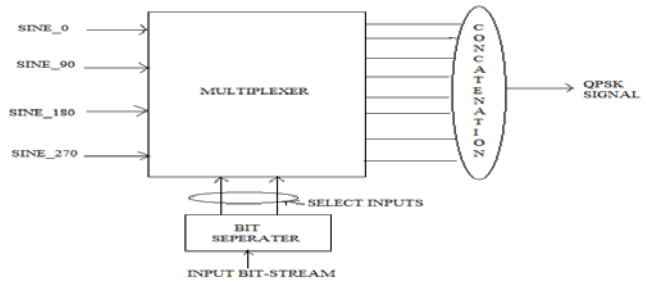

Figure 8. Elaboration of Proposed method -2 of QPSK modulator

IV. SIMULATION RESULTS

Figure 9 shows the RTL obtained by synthesizing Verilog HDL code for conventional QPSK modulator. Figure10 shows the simulator timing diagram, where odd and even data change from 00 to 01 and 11 to 10. Then the data obtained is multipled with carrier wave generator to produce I and Q phases and then added to both phases to generate QPSK signal. Here DDS is used and design 16 phases to generate sine and cosine wave.

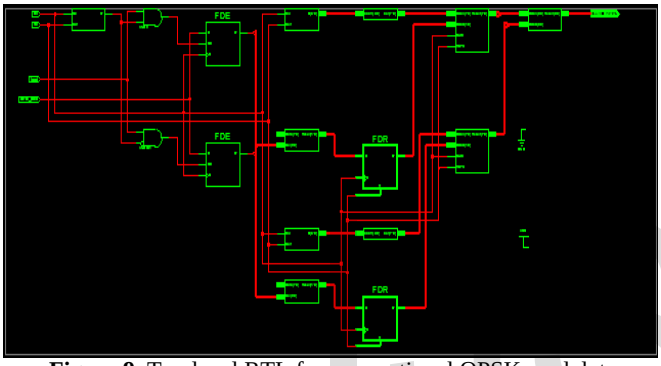

Figure 9. Top level RTL for conventional QPSK modulator

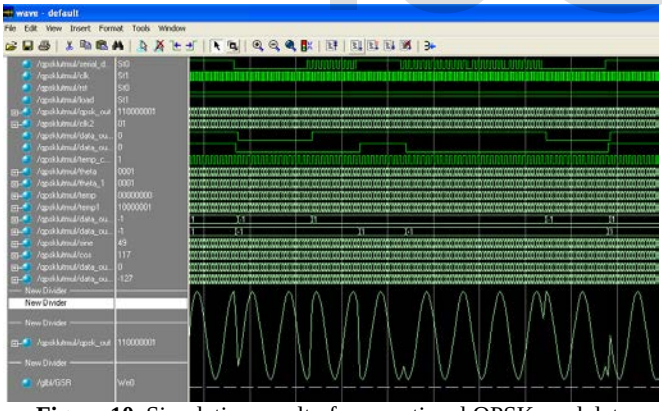

Figure 10. Simulation result of conventional QPSK modulator

Figure 11 represents the output of carry look-ahead adder where, a and b are the inputs which are 8-bit wide and cin is the carry input which should be zero for addition operation. s, p and g are the sum, carry generate and carry propagate respectively each of 8- bit width, cout is the output carry of one bit.

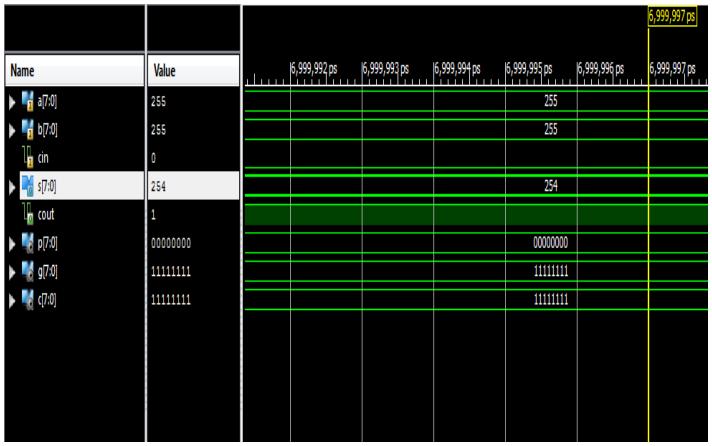

Figure 11. Carry look-ahead adder results

Here a and b represents the inputs to the Vedic multiplier each of 16 bits width and output of Vedic multiplier is out which is of 32 bits, and ca1,ca2,ca3 represents the intermediate carry outputs from the carry look ahead adders used in the design.

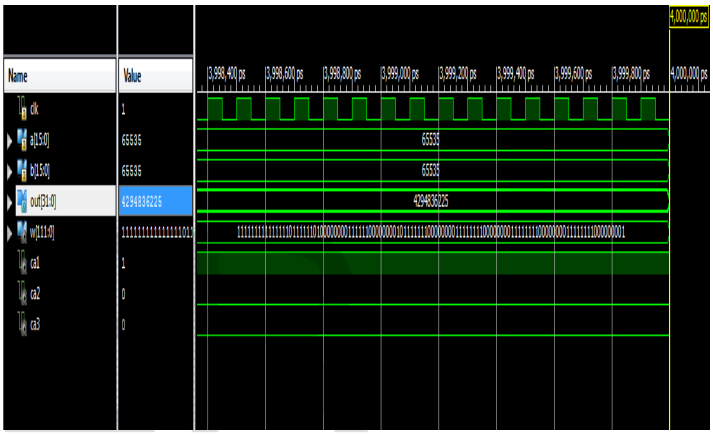

Figure 12. 16 bit Vedic multiplier result

This represents sine and cosine waveforms generated in Modelsim 6.1 version

Figure 13. Sine and cosine wave generation in Modelsim

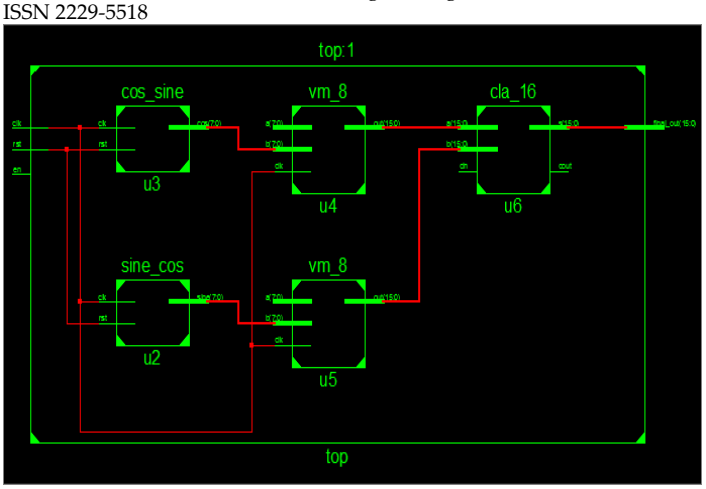

Figure 14. RTL schematic for proposed method-1 with AWGN.

This represents the final QPSK output in digital format generated using ISim inbuilt simulator present in Xilinx 14.7 version. final_out is the QPSK output and clk, rst, en and data_in are the inputs.

Figure 15. QPSK modulation for proposed method-1 in ISim simulator with AWGN.

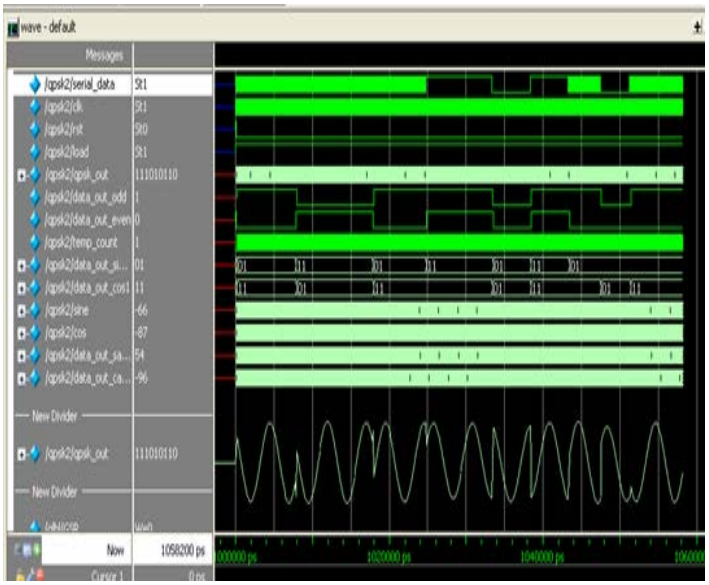

Figure 16. Simulation result of proposed QPSK Modulator 1 in Model simulator from mentor graphics EDA tool.

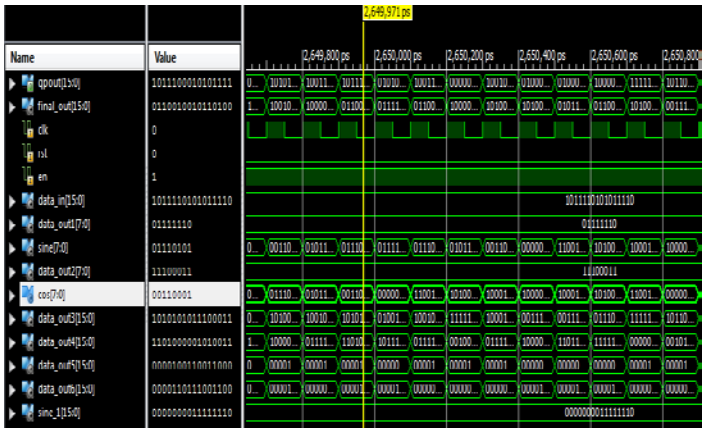

Figure 17. QPSK demodulation for proposed method-1 in ISim simulator with AWGN.

This represents the QPSK output generated by proposed method-2 using multiplexer concept.

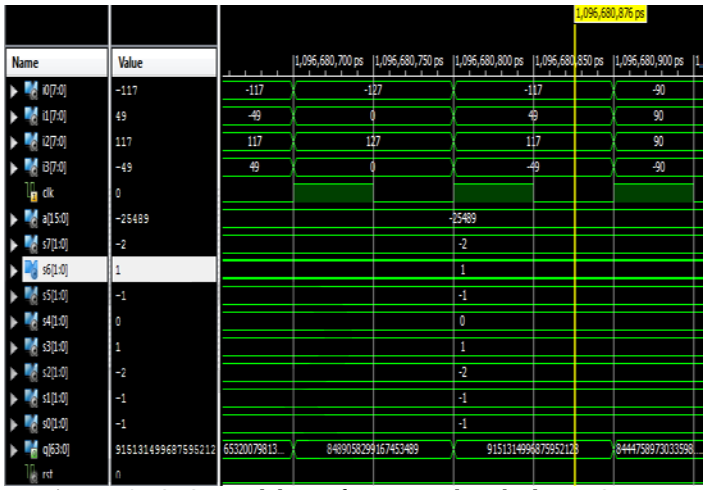

Figure 18. QPSK modulation for proposed method-2 in ISim simulator.

Figure 19 shows the RTL schematic diagram and Fig.20 shows the simulator timing diagram. Since the data for each QPSK phase is collected and stored in four different Read Only Memory (ROM) blocks. Once the four phases QPSK modulator data is collected from proposed QPSK modulator 1, conventional QPSK modulator is no longer required. A group of 2 bits is used to represent a phase in QPSK waveform. A total number of 50 data stored in each ROM to represent a phase in QPSK wave. Fig.8 shows the baseband data transition form 00, 01, 11 and 10.

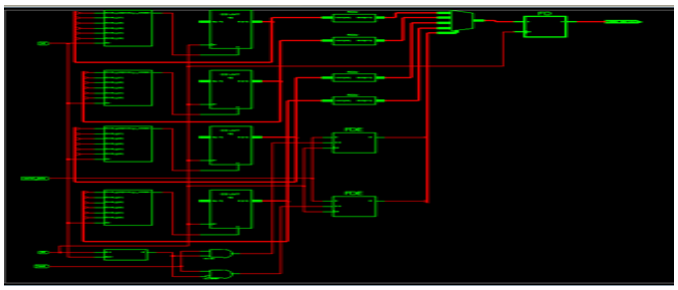

Figure 19. RTL schematic for proposed method-2

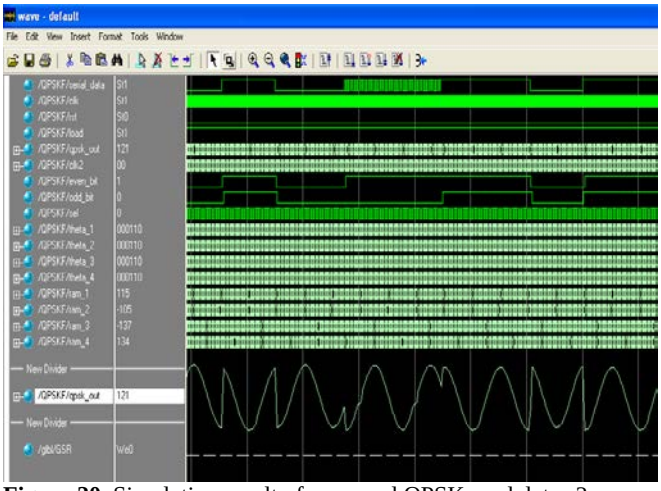

Figure 20. Simulation result of proposed QPSK modulator 2

FIR Low Pass Filter output designed using Hamming and Rectangular window in MATLAB.

The below Figure 21 represents the magnitude and phase response of Low Pass Filter designed using hamming windowing technique. Here, the cutoff frequency of the filter is 800 Hz approximately[12].

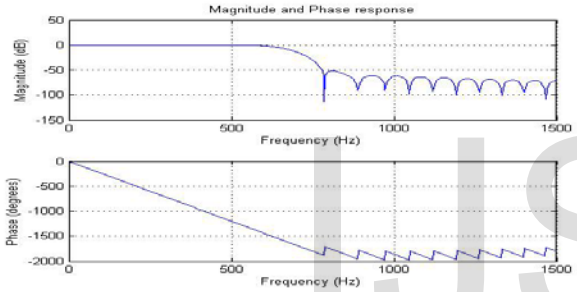

Figure 21. FIR Low pass filter output using Hamming window

Table 1: Filter Coefficients generated using Hamming window

0.0010	0.0011	-0.0008	-0.0024	0.0002	0.0045	0.0021	-0.0069	-0.0072
0.0079	0.0156	-0.0048	-0.0271	-0.0059	-0.0399	0.0298	-0.0519	-0.0831
0.0603	0.3097	0.4357	0.3097	0.0603	-0.0831	-0.0519	0.0298	-0.0399
-0.0059	-0.0271	-0.0048	0.0156	0.0079	-0.0072	-0.0069	0.0021	0.0045
0.0002	-0.0024	-0.0008	0.0011	0.0010				

Table 2: Filter Coefficients generated using rectangular window

0.008	0.0011	-0.0002	-0.0018	-0.0015	0.0017	0.0042	0.0012	-0.0058	-0.0073	0.0023	0.013
0.0085	-0.0122	-0.0236	-0.0032	0.0323	0.0345	-0.0182	-0.0740	-0.0428	0.1074	0.2939	0.378
0.2939	0.1074	-0.0428	-0.0740	-0.0182	0.0345	0.0323	-0.0032	-0.0032	-0.0236	-0.0122	0.0085
0.013	0.0023	-0.0073	-0.0058	0.0012	0.0042	0.0017	-0.0015	-0.0018	-0.0002	0.0011	0.008

A. HARDWARE IMPLEMENTATION

The designed QPSK modulator using Vedic multiplier and carry look-ahead adder is implemented on Spartan3 FPGA kit and the simulated digital output of QPSK is converted to analog waveform by connecting C4 to C21 which converts digital format into analog waveform and this analog output is seen in CRO as shown in the Figure 21and 22.

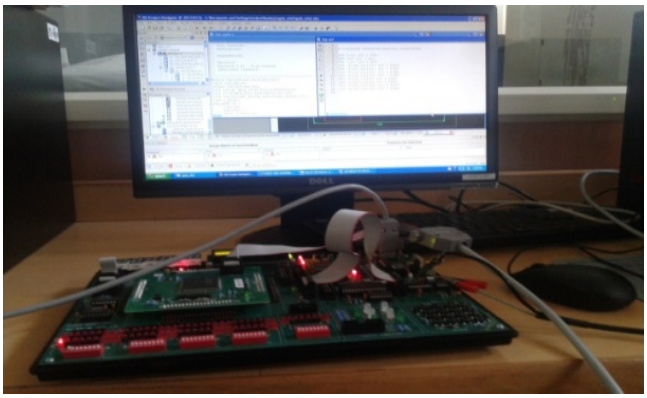

Figure 21 FPGA implementation of QPSK modem proposed method-1

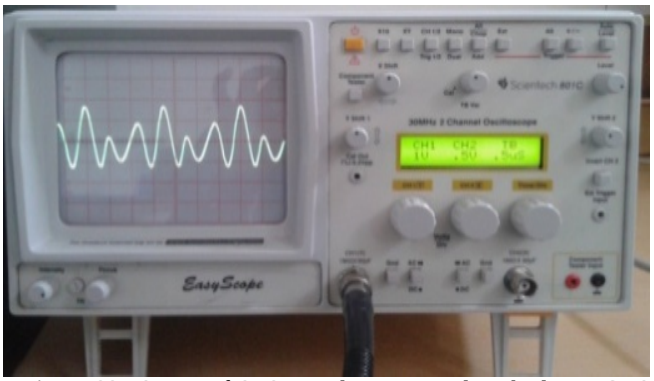

Figure 22. Output of QPSK modem proposed method-1 on CRO

The QPSK modulation technique using multiplexer concept is implemented on Spartan3 FPGA board Atlys sparten-6 FPGA kit and the analog output waveform is observed in CRO shown in Fig 23 and Fig 24.

Figure 23. FPGA Implementation of QPSK modulation proposed method -2

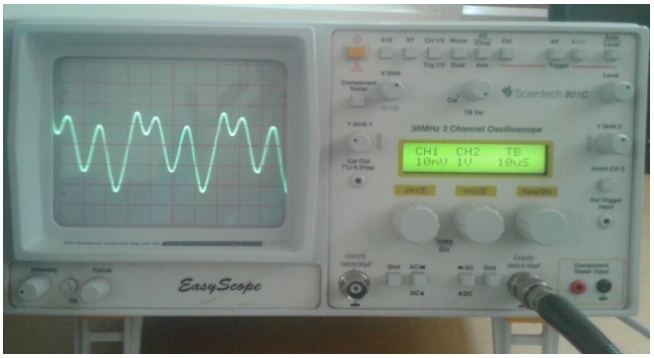

Figure 24. Output of QPSK modulation proposed method-2 on CRO

Table 3: Comparison of three modulation techniques in terms of frequency and AWGN on Spartan-3 FPGA board.

Method	Maximum frequency of operation
Conventional QPSK method	146.803 MHZ
Proposed method-1	252.277 MHZ without AWGN 275.256 MHZ with AWGN
Proposed method -2	343.389 MHZ

Table 4: Comparison of three modulation techniques in terms of Frequency and AWGN on Spartan-6(Atlys) FPGA board.

Method	Maximum frequency of operation
Conventional QPSK method	291.911 MHZ
Proposed method-1	438.779 MHZ without AWGN 475.556 MHZ with AWGN
Proposed method -2	446.100 MHZ

V CONCLUSIONS

With the proposed methods 1 and 2 compared to conventional modulator design (using arithmetic adder and multiplier respectively) there is a great improvement in the throughput. In proposed method QPSK modulator-1 Multiplier and LUT's are used for carrier generation and arithmetic multiplier, arithmetic adder is replaced by Vedic multiplier and carry look-ahead adder respectively. In second method multiplexer concept is used to design QPSK modulator. All these methods are successfully simulated on Xilinx ISE 14.7 software and implemented in FPGA Spartan-3 board as well as Spartan 6 kit. The power consumption, timing and area utilization achieved in the proposed method QPSK modulator-2 also gives a high throughput as shown in Table. The FIR LPF for proposed method-1 QPSK demodulator is designed by using Hamming and rectangular windowing technique in MATLAB with AWGN and demodulation results are obtained and the whole module is implemented on Spartan-3 XC3S400 and Spartan-6(ATLYS) FPGA hardware. The designed QPSK modem using proposed method-1 and proposed method-2 gives better performance over conventional QPSK method as discussed and also these designed QPSK modem gives better results when implemented on Spartan-6(ATLYS) FPGA board compared to Spartan-3 FPGA board.

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Parts of this paper were presented at the IEEE 2015 IC-SSS Conference [18]. In this paper [18], performance improvement of QPSK modem was implemented in FPGA without considering the noise element and conventional multipliers and adder were used. In the current paper, performance improvement of QPSK modem is being implemented in FPGA by adding Additive White Gaussian Noise (AWGN) and replacing conventional multipliers and adder by Vedic array multipliers and carry look-ahead adder.